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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/781,788 | 02/20/2004 | Takefumi Yoshikawa | 60188-777 | 6637 |

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| EXAMINER | |
|---|---|
| NGUYEN, LINH V | |

| ART UNIT | PAPER NUMBER |
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| 2819 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/781,788 | YOSHIKAWA, TAKEFUMI | |
| | Examiner | Art Unit | |
| | Linh V. Nguyen | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,11,13 and 15* is/are rejected.

7)☒ Claim(s) *3,4,7-10,12,14 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to communication filed on 2/20/2004. Claims 1 – 18 are pending on this application.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 5 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi et al. U.S. patent No. 6,370,162.

Regarding claim 1, Fig. 1 of Takahashi et al. discloses a data transmitting/receiving device, comprising: a serial-parallel conversion circuit (1) for converting received first serial data (D1) to first parallel data (S1); a data selection circuit (3) for selecting any one of the first parallel data (S2) and externally-supplied second parallel data (S3; S3 is an external supply data because buffer 2 – 2 is an external circuit from buffer 2 – 1; therefore S3 is an external parallel data from parallel data S2) and outputting the selected data (S4) ; and a parallel-serial conversion circuit (4) for converting the first or second parallel data (S2 or S3) output from the data selection circuit (3) to second serial data (Dout) which is to be transmitted.

Regarding claim 2, wherein the parallel-serial conversion circuit (4) operates in synchronization with the serial-parallel circuit (1) when the data selection circuit (3)

selects the first parallel data (S2; output of buffer 2 – 1 is selected; See Fig. 7A – 7F for discloses synchronization Ckin and Ckout for S/P converter 1 and P/S converter 4 when output of buffer 2 – 1 is selected, which is S2)

Regarding claim 5, Fig. 1 of Takahashi et al. discloses a data transmitting/receiving device, comprising: a serial-parallel conversion circuit (1, 2) for converting received first serial data (D1) to first parallel data (S2); a data processing circuit (2 – 2) for outputting second parallel data (S3); a control circuit for stopping the operation of the data processing circuit (this is inherent to Fig. 1 of Takahashi et al. because every electrical circuit must have a control circuit for stopping the operation such as power off the circuit for stopping the operation of any electrical circuit) ; a data selection circuit (3) for selecting any one of the first parallel data (S2) and the second parallel data (S3) and outputting the selected data (S4); and a parallel-serial conversion circuit (4) for converting the first or second parallel data (S4) output from the data selection circuit (3) to serial data (Dout) which is to be transmitted.

Regarding claim 6, the claim incorporated the same subject matter as of claim 2 above, and rejected along the same rationale.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 11, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. as applied to claims 1 and 5 above, and further in view of Misutani U.S. patent No. 6,476,738.

Regarding claim 11, Takahashi et al. as applied to claim 1 above, disclosed every aspect of claimed invention except for a latch circuit for storing received first serial data.

Fig. 1 of Misutani discloses a serial/parallel (3, 6) and parallel/serial (7) converters; wherein serial/parallel converter comprising a latch circuit (3) for storing received first serial data (Din).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate latching circuit of Misutani into Takahashi et al. for the purpose to providing high speed storages for high speed operation without increase the cost of circuitry (Misutani' s col. 2 lines 36 – 42).

Regarding claims 13 and 15, Takahashi et al. as applied to claim 5 above, disclosed every aspect of claimed invention except for a latch circuit for storing received first serial data.

Fig. 1 of Misutani discloses a serial/parallel (3, 6) and parallel/serial (7) converters; wherein serial/parallel converter comprising a latch circuit (3) for storing received first serial data (Din).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate latching circuit of Misutani into Takahashi et al. for

the purpose to providing high speed storages for high speed operation without increase the cost of circuitry (Misutani' s col. 2 lines 36 – 42).

***Allowable Subject Matter***

6. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art does not teach a clock adjustment circuit for receiving a first clock signal and the first serial data and adjusting the first clock signal to output a second clock signal which is in synchronization with the first serial data, wherein the serial-parallel conversion circuit operates in synchronization with the second clock signal.

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art does not teach a clock selection circuit for selecting any one of the first clock signal and the second clock signal and inputting the selected clock signal to the parallel-serial conversion circuit, wherein: when the data selection circuit selects the first parallel data, the clock selection circuit selects the second clock signal; and when the data selection circuit selects the second parallel data, the clock selection circuit selects the first clock signal.

Claims 7 - 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art does not teach a clock adjustment

circuit for receiving a first clock signal and the first serial data and adjusting the first clock signal to output a second clock signal which is in synchronization with the first serial data, wherein the serial-parallel conversion circuit operates in synchronization with the second clock signal.

Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art does not teach a clock adjustment circuit for receiving a first clock signal and the first serial data and adjusting the first clock signal to output a second clock signal which is in synchronization with the first serial data, wherein the latch circuit and the serial-parallel conversion circuit operate in synchronization with the second clock signal.

Claim 14, 16, 17 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art does not teach a clock a clock adjustment circuit for receiving a first clock signal and the first serial data and adjusting the first clock signal to output a second clock signal which is in synchronization with the first serial data, wherein the latch circuit and the serial-parallel conversion circuit operate in synchronization with the second clock signal.

***Contact Information***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571)

272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Rexford Barnie can be reached at (571) 272-7492. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

8/18/07

Linh Van Nguyen

Art Unit 2819